

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

KALYAN MUTHUKUMAR, ET AL.

Application No.:

Filed:

For: **Resource-Aware Scheduling for Compilers**

Art Group:

Examiner:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed for applications filed after June 30, 2003). This IDS and IDS Citation Form are being submitted concurrently with the Utility Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

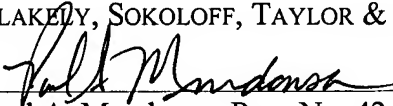
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Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: March 24, 2004


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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.


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03-24-04

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				Application Number	
				Filing Date	
				First Named Inventor	Kalyan Muthukumar
				Art Unit	
				Examiner Name	
				Attorney Docket Number	42P18140
Sheet	1	of	1		

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ²
	1	Bharadwaj et. al, "The Intel IA-64 Compiler Code Generator", IEEE 0272-1732/00, 2000		
	2	Kastner and Winkel, "ILP-based Instruction Scheduling for IA-64", Proceedings of the ACM SIGPLAN Workshop on Languages, Compilers and Tools for Embedded Systems, Utah, 2001, ACM 1-58113-425-8/01/06		
	3	K. Cooper et al., "An Experimental Evaluation of List Scheduling", Department of Computer Science, Rice University, Houston, Texas		
	4	Deitrich et. al, "Speculative Hedge: Regulating Compile-Time Speculation Against Profile Variations," Proceedings of the 29th Annual International Symposium on Microarchitecture, December 2-4, pp. 70-79, 1996		

Examiner Signature		Date Considered	
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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Applicant's unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08B (08-03) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 08/11/2003.
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